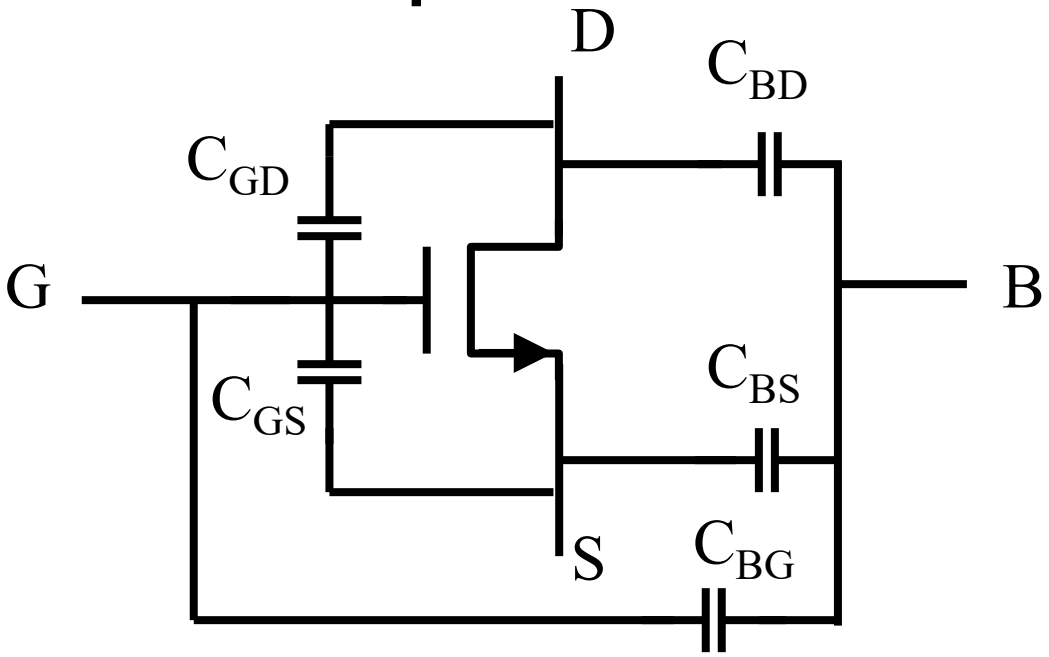
EE 435

Lecture 32

- String DACs
- Switches
- Current Steering DACs

Review from Last Lecture

Parasitic Capacitance Summary



	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$CoxWL_D + 0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S +(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Review from Last Lecture

R-String DAC

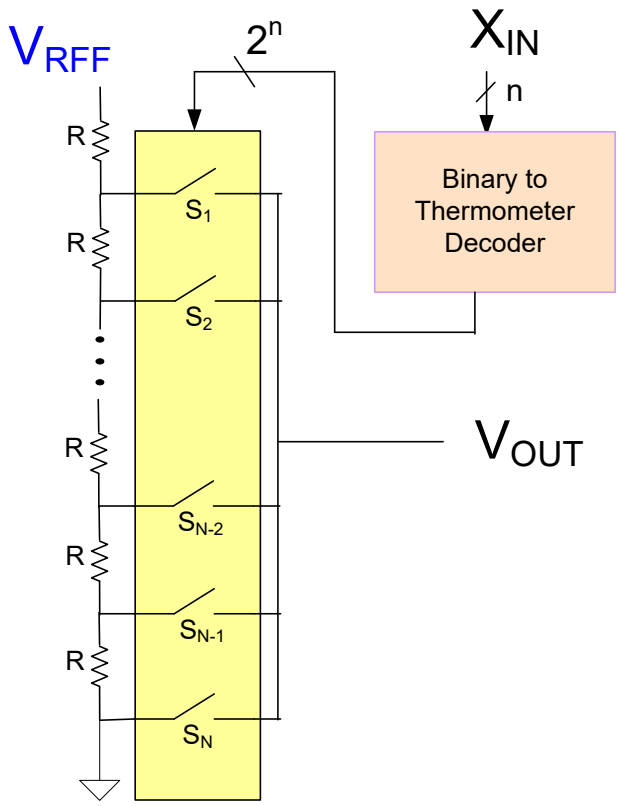
If all components are ideal, performance of the R-string DAC is that of an ideal DAC!

Key Properties of R-String DAC

- One of the simplest DAC architectures
- R-string DAC is inherently monotone

Possible Limitations or Challenges

- Binary to Thermometer Decoder (BTTD) gets large for n large
- Logic delays in BTTD may degrade performance
- Matching of the resistors may not be perfect
  - Local random variations
  - Gradient effects
- How can switches be made ?

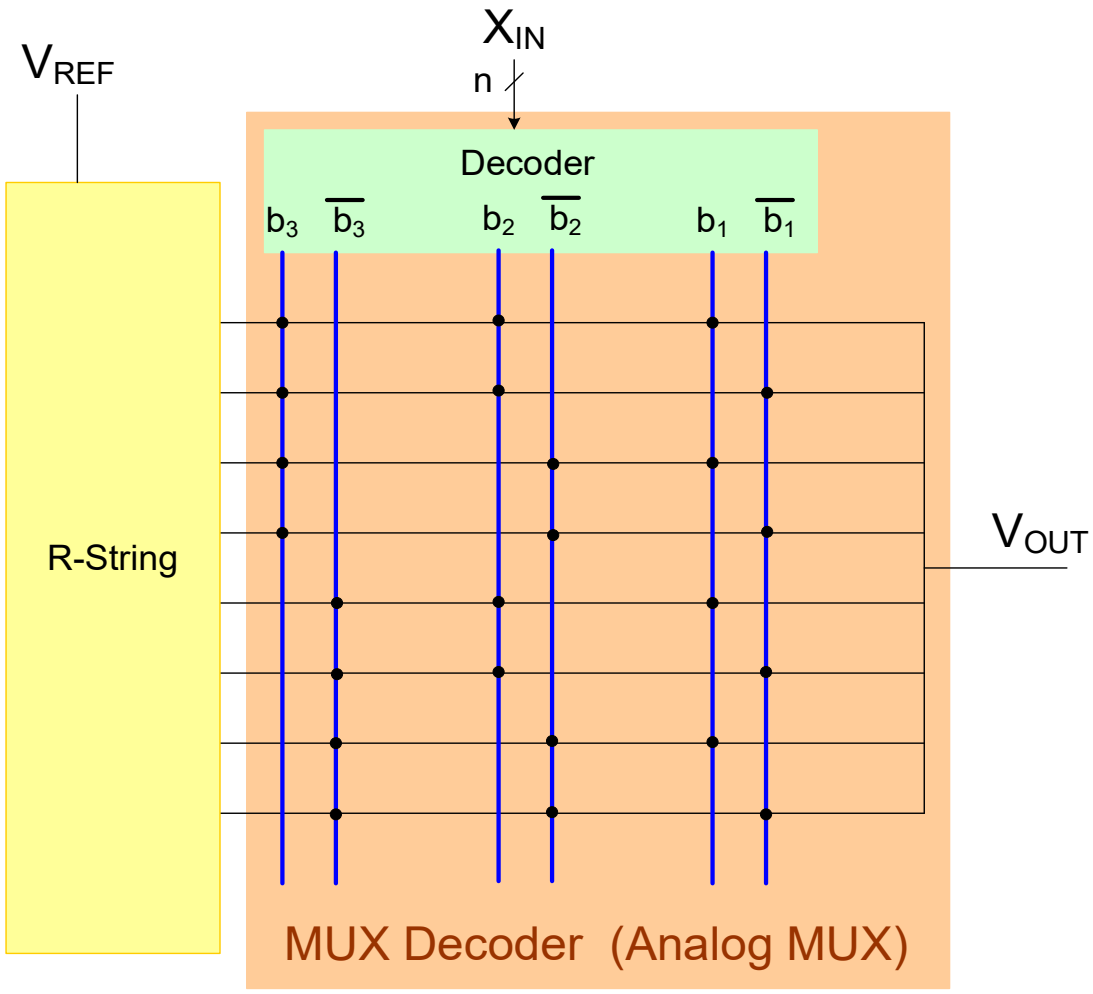


Review from Last Lecture

R-String DAC

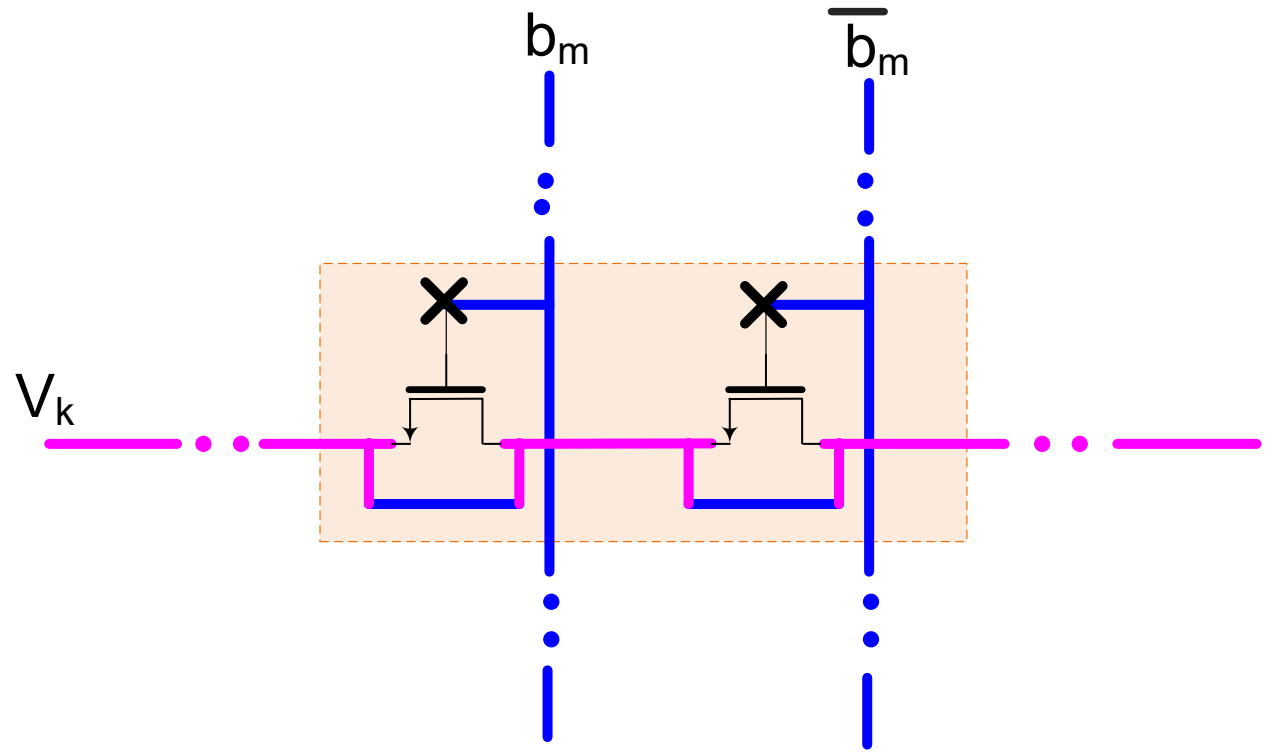
Tree-Decoder Layout/Architecture

Each intersection is a reserved site for a switch



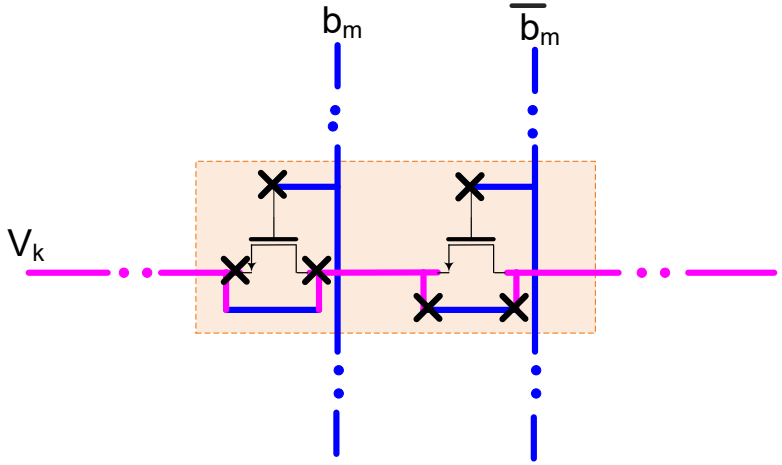
Review from Last Lecture

Uncontacted Row-Column Structure

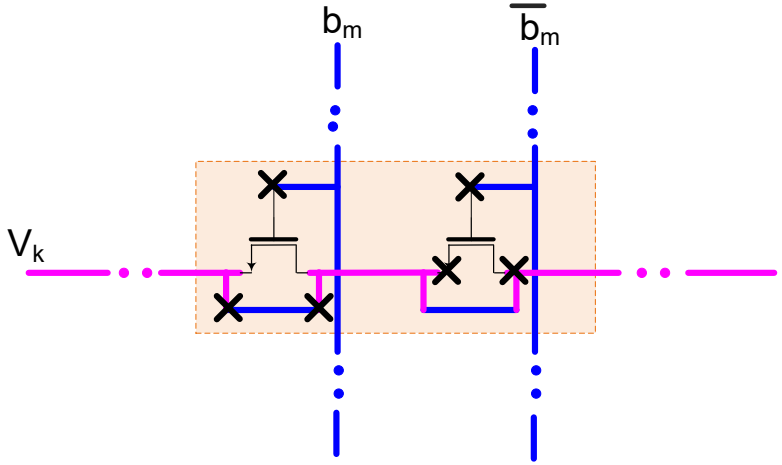


Review from Last Lecture

Row-Column Structure with Contacts Added



OR



Programmed entirely with the contact mask

What DAC Architectures are Actually Used?

Listing from Texas Instruments March 1 2023

String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

6.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V, –40°C to +105°C range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
Resolution			16			Bits
Relative accuracy	Measured by line passing through codes 485 and 64714	DAC8560A, DAC8560C		±4	±12	LSB
		DAC8560B, DAC8560D		±4	±8	LSB
Differential nonlinearity	16-bit Monotonic			±0.5	±1	LSB
Zero-code error	Measured by line passing through codes 485 and 64714.			±5	±12	mV
Full-scale error				±0.2	±0.5	% of FSR
Gain error				±0.05	±0.2	% of FSR
Zero-code error drift				±4		µV/°C
Gain temperature coefficient	V_{DD} = 5 V			±1		ppm of FSR/°C
	V_{DD} = 2.7 V			±3		
PSRR	Power supply rejection ratio	Output unloaded		1		mV/V
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		V_{REF}	V
Output voltage settling time	To ±0.003% FSR, 0200h to FD00h, R_L = 2 kΩ, 0 pF < C_L < 200 pF			8	10	µs
	R_L = 2 kΩ, C_L = 500 pF			12		
Slew rate				1.8		V/µs
Capacitive load stability	R_L = ∞			470		pF
	R_L = 2 kΩ			1000		
Code change glitch impulse	1 LSB change around major carry			0.15		nV-s
Digital feedthrough	SCLK toggling, $\overline{SYNC}$ high			0.15		nV-s
DC output impedance	At mid-code input			1		Ω
Short-circuit current	V_{DD} = 5 V			50		mA
	V_{DD} = 3 V			20		
Power-up time	Coming out of power-down mode V_{DD} = 5 V			2.5		µs
	Coming out of power-down mode V_{DD} = 3 V			5		
AC PERFORMANCE(2)						
SNR	T_A = 25°C, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			88		dB
THD				–77		dB
SFDR				79		dB
SINAD				77		dB
DAC output noise density	T_A = 25°C, at mid-code input, f_{OUT} = 1 kHz			170		nV/√Hz
DAC output noise	T_A = 25°C, at mid-code input, 0.1 Hz to 10 Hz			50		μV_{PP}

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design and characterization, not production tested.

The DAC 8560

What is the INL performance of this DAC?

ENOB (from INL)?

What would be the SNR if only quantization noise is present?

SNR - = 6n+1.76

What is the spectral performance?

ENOB (rel to quantization noise)?

6.5 Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V, –40°C to +105°C range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
Resolution			16			Bits
Relative accuracy	Measured by line passing through codes 485 and 64714	DAC8560A, DAC8560C		±4	±12	LSB
		DAC8560B, DAC8560D		±4	±8	LSB
Differential nonlinearity	16-bit Monotonic			±0.5	±1	LSB
Zero-code error	Measured by line passing through codes 485 and 64714.			±5	±12	mV
Full-scale error				±0.2	±0.5	% of FSR
Gain error				±0.05	±0.2	% of FSR
Zero-code error drift				±4		µV/°C
Gain temperature coefficient	V_{DD} = 5 V			±1		ppm of FSR/°C
	V_{DD} = 2.7 V			±3		
PSRR	Power supply rejection ratio	Output unloaded		1		mV/V
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		V_{REF}	V
Output voltage settling time	To ±0.003% FSR, 0200h to FD00h, R_L = 2 kΩ, 0 pF < C_L < 200 pF			8	10	µs
	R_L = 2 kΩ, C_L = 500 pF			12		
Slew rate				1.8		V/µs
Capacitive load stability	R_L = ∞			470		pF
	R_L = 2 kΩ			1000		
Code change glitch impulse	1 LSB change around major carry			0.15		nV-s
Digital feedthrough	SCLK toggling, $\overline{SYNC}$ high			0.15		nV-s
DC output impedance	At mid-code input			1		Ω
Short-circuit current	V_{DD} = 5 V			50		mA
	V_{DD} = 3 V			20		
Power-up time	Coming out of power-down mode V_{DD} = 5 V			2.5		µs
	Coming out of power-down mode V_{DD} = 3 V			5		
AC PERFORMANCE(2)						
SNR	T_A = 25°C, BW = 20 kHz, V_{DD} = 5 V, f_{OUT} = 1 kHz, 1st 19 harmonics removed for SNR calculation			88		dB
THD				–77		dB
SFDR				79		dB
SINAD				77		dB
DAC output noise density	T_A = 25°C, at mid-code input, f_{OUT} = 1 kHz			170		nV/√Hz
DAC output noise	T_A = 25°C, at mid-code input, 0.1 Hz to 10 Hz			50		μV_{PP}

(1) Linearity calculated using a reduced code range of 485 to 64714; output unloaded.
(2) Ensured by design and characterization, not production tested.

The DAC 8560

What is the INL performance of this DAC? ±12LSB

ENOB (from INL)? 11.5

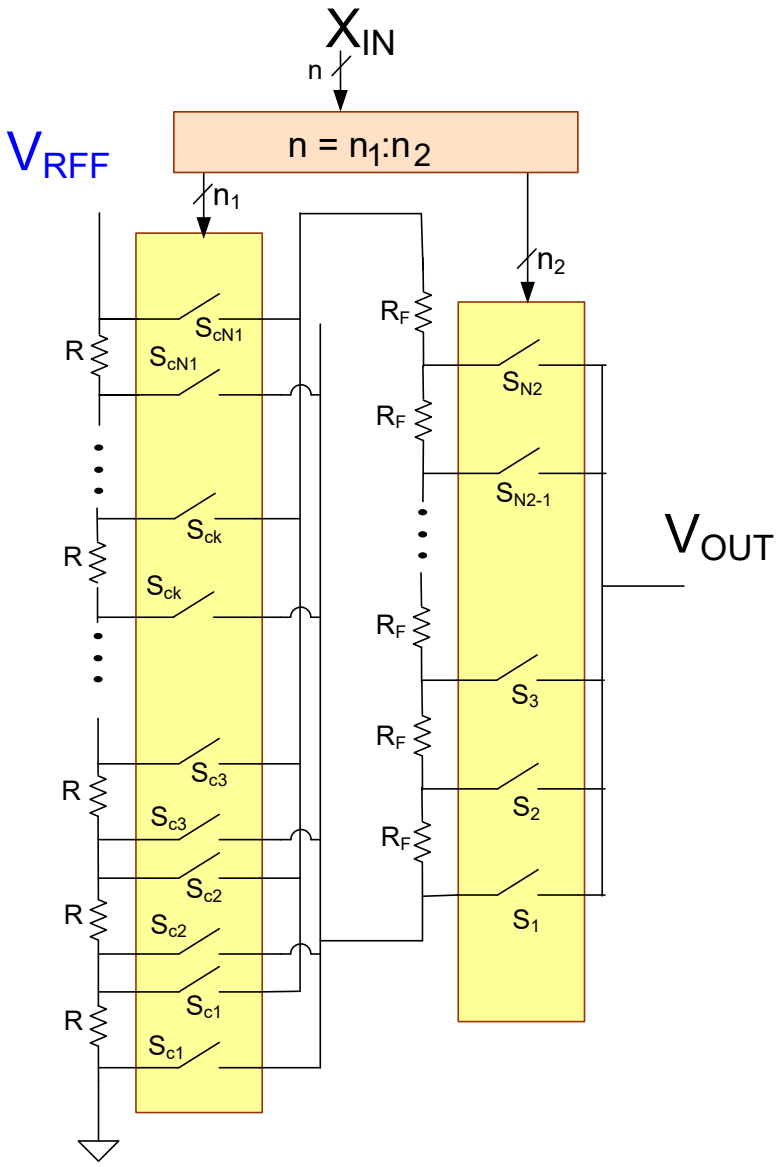
What would be the SNR if only quantization noise is present?

SNR - = 6n+1.76 97.6

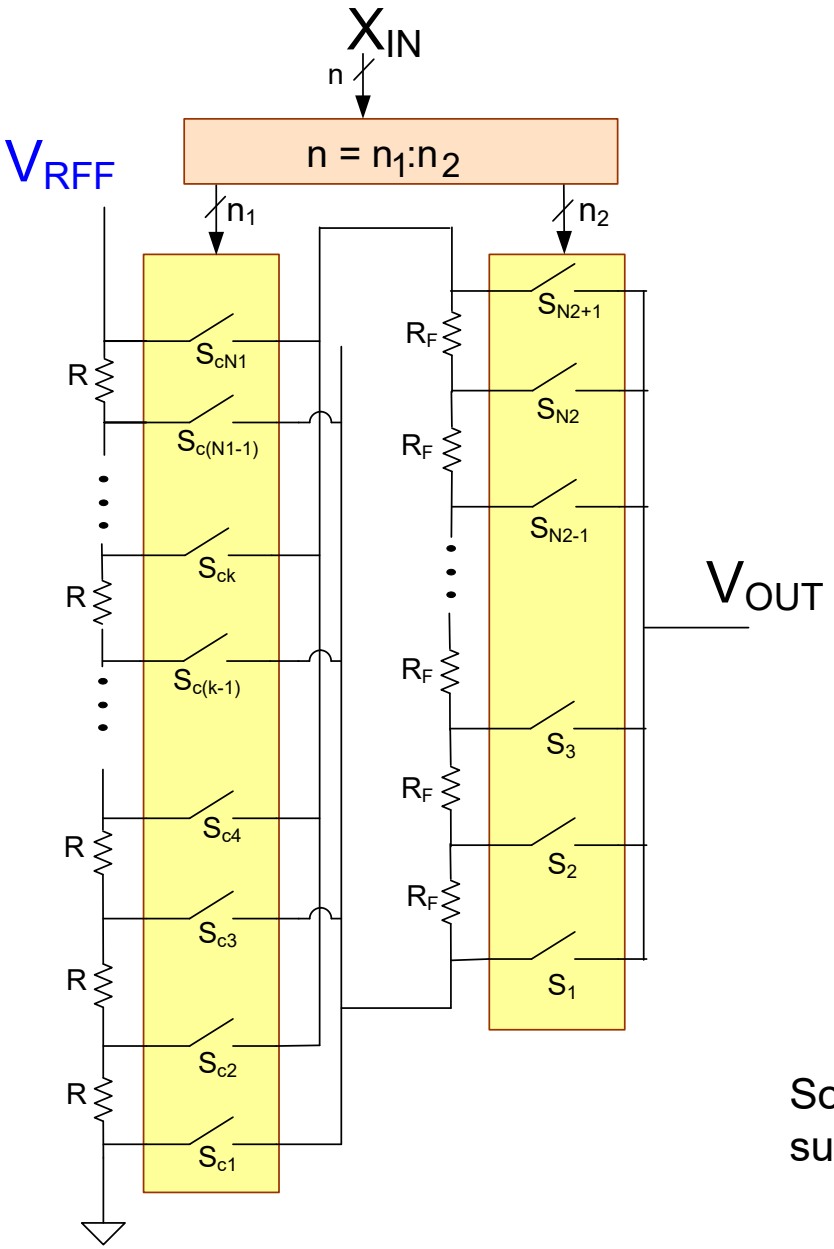
What is the spectral performance? SINAD = 77dB

ENOB (rel to quantization noise)? 12.6

R-String DAC

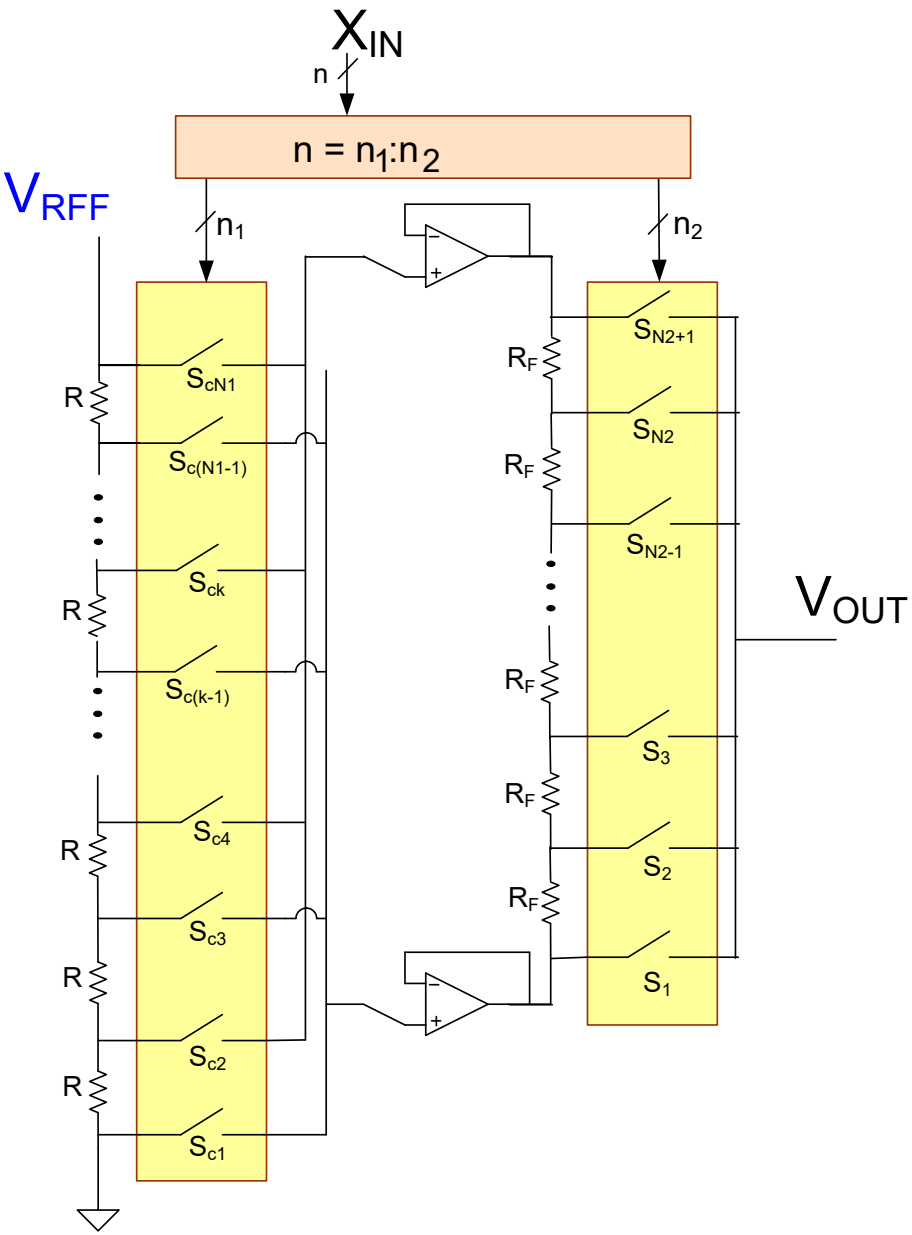

X_IN
n
n = n1:n2
V_RFF
n1
n2
R
S_cN1
S_ck
S_c3
S_c2
S_c1
R_F
S_N2
S_N2-1
S_3
S_2
S_1
V_OUT

R-String DAC

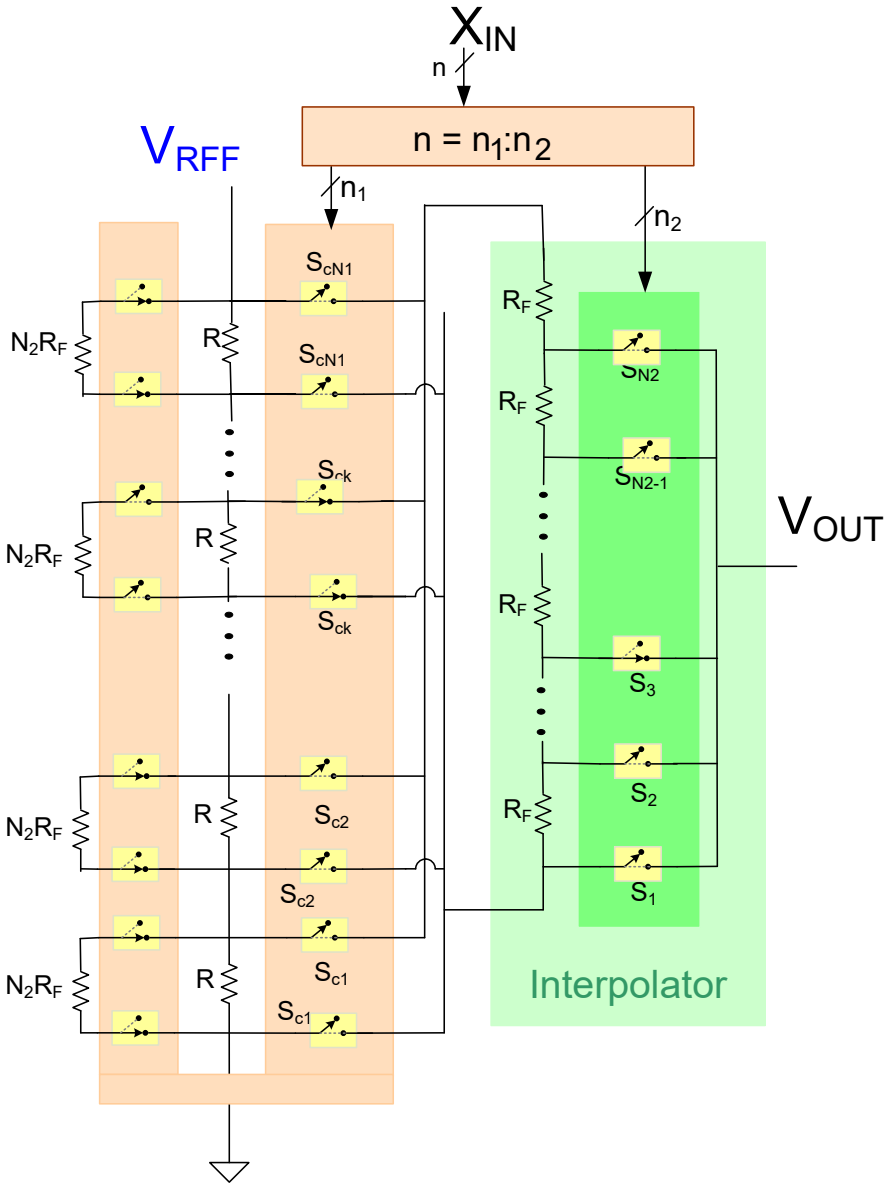


Sometimes termed sub-divider, sub-range or dual-string DAC

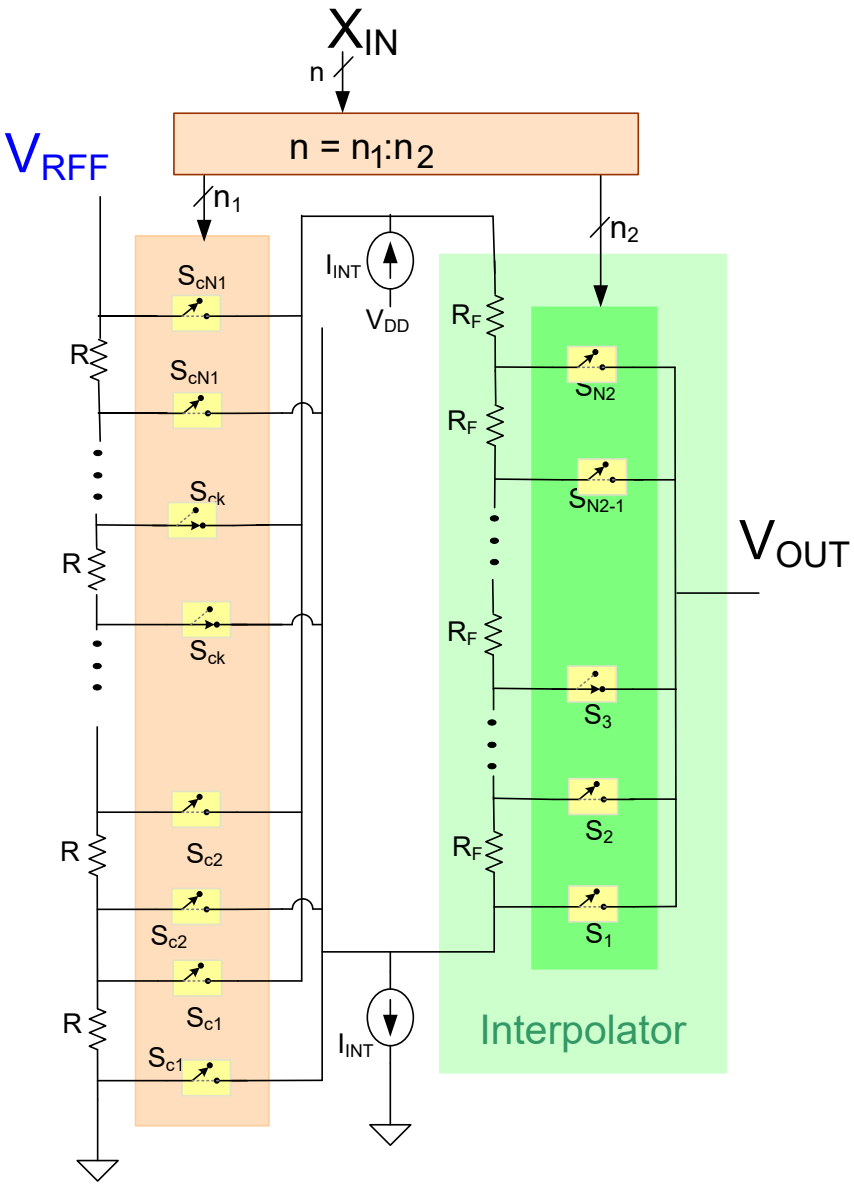
R-String DAC


X_IN
n
n = n1:n2
V_RFF
n1
n2
S_N2+1
S_N2
S_N2-1
S_3
S_2
S_1
S_cN1
S_c(N1-1)
S_ck
S_c(k-1)
S_c4
S_c3
S_c2
S_c1
R_F
R
V_OUT

R-String DAC


X_IN
n
n = n1:n2
V_RFF
n1
n2
S_cN1
S_cN1
N2R_F
R
S_ck
S_ck
N2R_F
R
N2R_F
R
S_c2
S_c2
N2R_F
R
S_c1
S_c1
R_F
R_F
R_F
R_F
S_N2
S_N2-1
S_3
S_2
S_1
V_OUT
Interpolator

R-String DAC


X_IN
n
n = n1:n2
V_RFF
n1
n2
I_INT
V_DD
S_cN1
R
S_ck
S_c2
S_c1
R_F
S_N2
S_N2-1
S_3
S_2
S_1
V_OUT
Interpolator

R-String DAC

Will now look at a classic paper that discusses several key strategies for building string DACs

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 25, NO. 6, DECEMBER 1990

A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

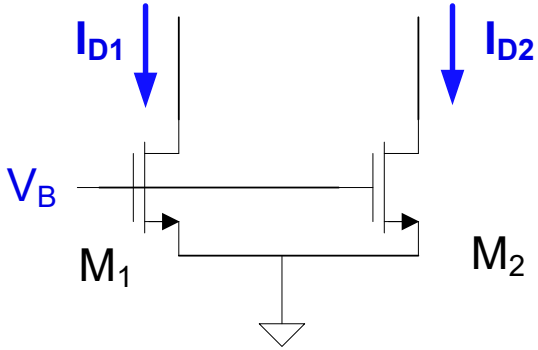
MARCEL J. M. PELGROM, MEMBER, IEEE

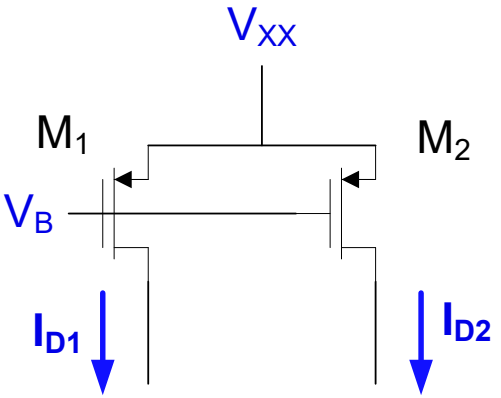
Though somewhat dated, results are particularly relevant

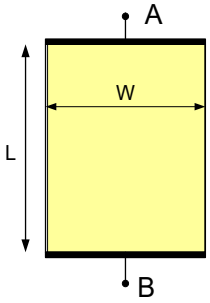
Most data converter architectures require good matching of a large number of one or more types of components

Some key background information relating to stastical characterization of data converters will be discussed to better understand concepts discussed in this paper

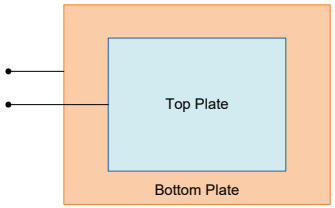
Matching Properties of Circuit Components



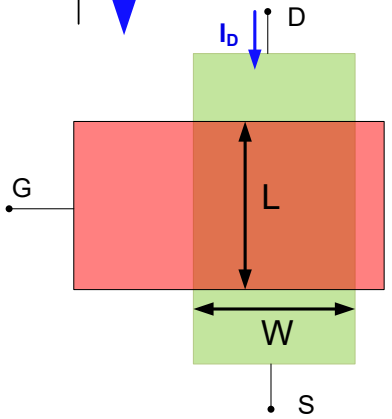




$$\sigma^2_{\frac{R}{R_N}} \cong \frac{A^2_{\rho N}}{WL}$$

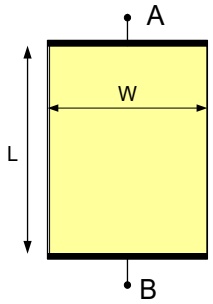


$$\sigma^2_{\frac{C_R}{C_N}} \cong \frac{A^2_C}{A_{TOP}}$$

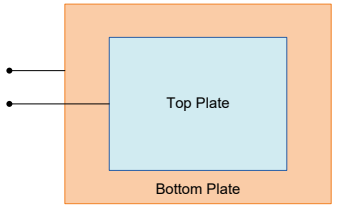


$$\sigma^2_{\frac{I_D}{I_{DN}}} \cong \frac{1}{WL}\left(\frac{4}{V^2_{EB}}A^2_{VT0} + A^2_{COX} + A^2_{\mu}\right)$$

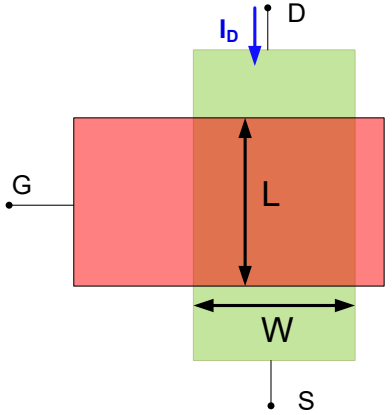
Matching Properties of Circuit Components



$$\sigma^2_{\frac{R}{R_N}} \cong \frac{A^2_{\rho N}}{WL}$$



$$\sigma^2_{\frac{C_R}{C_N}} \cong \frac{A^2_C}{A_{TOP}}$$

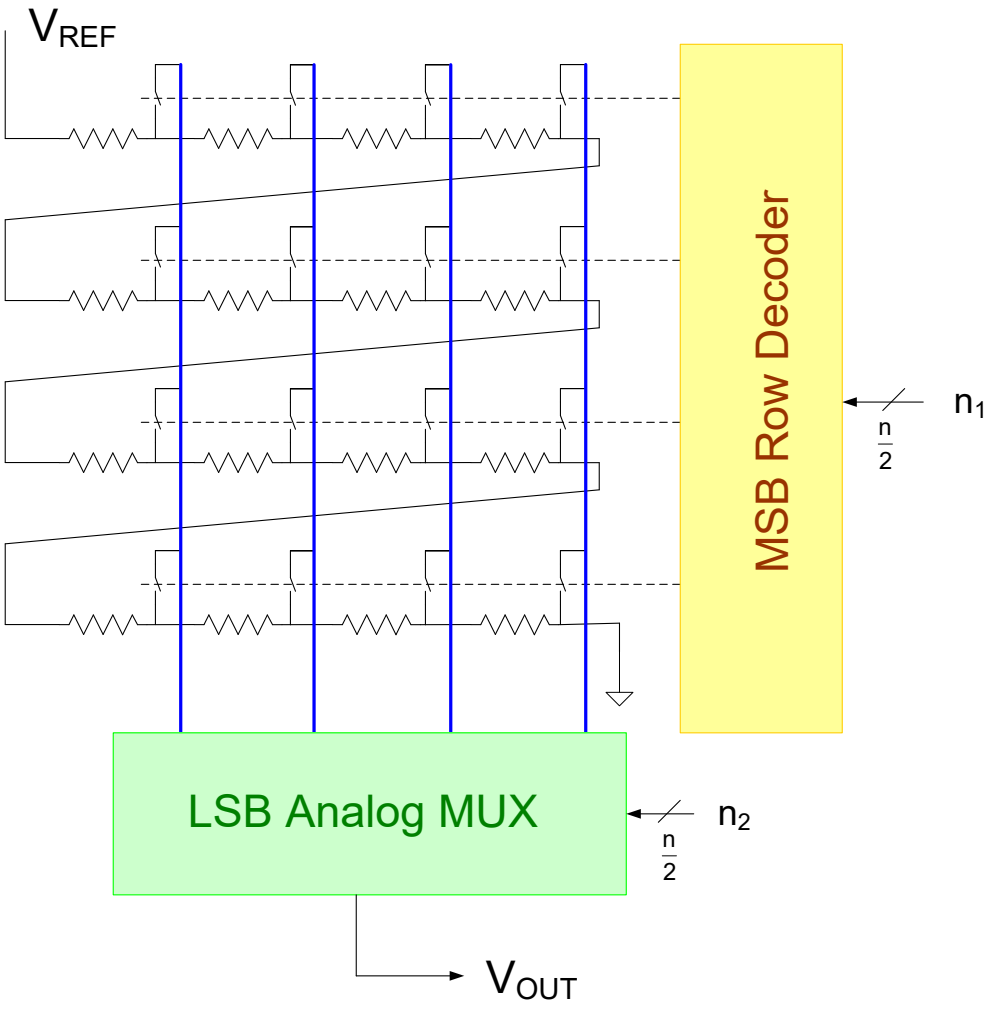


$$\sigma^2_{\frac{I_D}{I_{DN}}} \cong \frac{1}{WL}\left(\frac{4}{V^2_{EB}} A^2_{VT0} + A^2_{COX} + A^2_{\mu}\right)$$

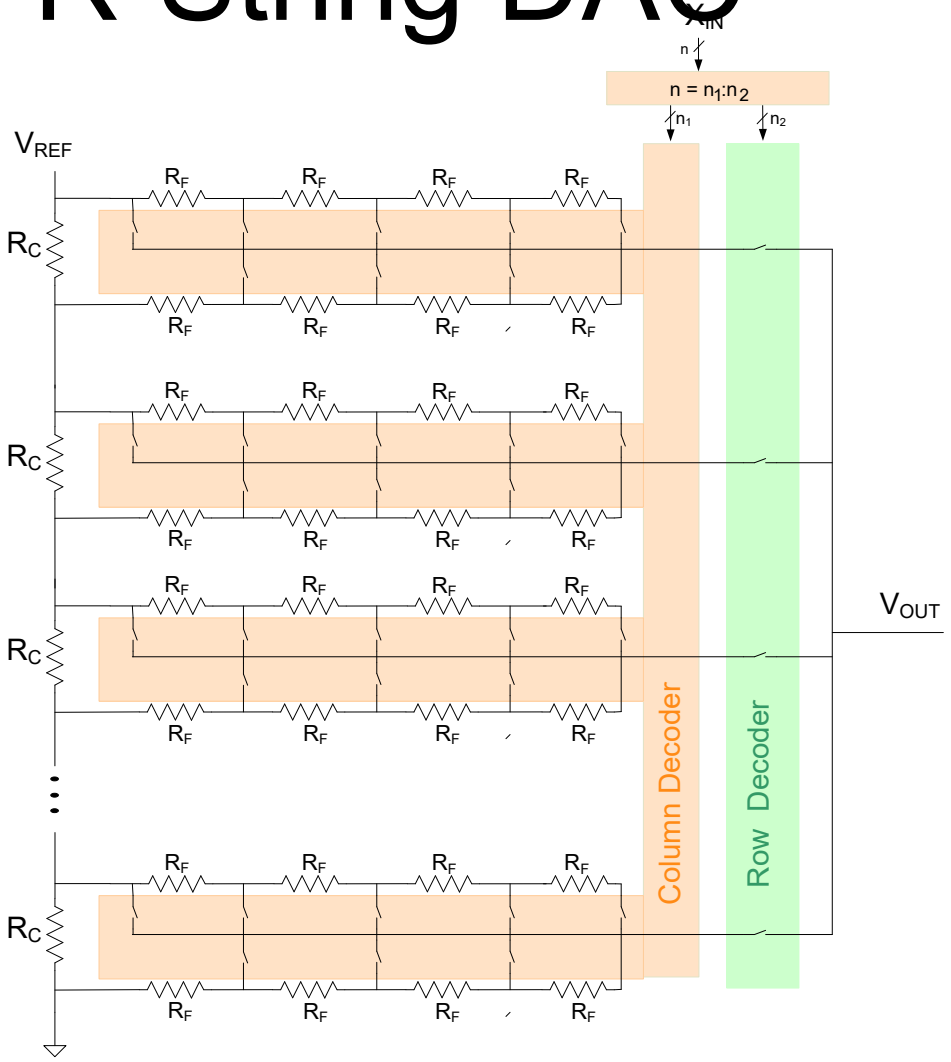
- If edge roughness effects are neglected, standard deviation of components $\sigma_{\frac{X}{X_N}}$ proportional to reciprocal of the square root of area of component
- INL and DNL of most data converters (at low f) depends upon matching characteristics of basic circuit components
- Often INL and DNL proportional to standard deviation of components
- Each additional bit of ENOB generally requires a factor of 2 reduction in σ

Each additional bit of ENOB generally requires a factor of 4 increase in area in matching critical circuits !!

R-String DAC



R-String DAC



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 25, NO. 6, DECEMBER 1990

Note Dual Ladder is used !

A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

MARCEL J. M. PELGROM, MEMBER, IEEE

A 10-b 50-MHz CMOS D/A converter with 75-Ω buffer - Get It@ISU

MJM **Pelgrom** - IEEE Journal of Solid-State Circuits, 1990 - ieeexplore.ieee.org

Abstracf -A 10-b 50-MHz digital-to-analog (D/A) converter is pre- sented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A ...

Cited by 45 - Related articles - Web Search - All 2 versions

Cited by 51 (4/5/10) Cited by 109 (4/5/16)
Cited by 94 (4/6/14) Cited by 130 (4/24/19)
Cited by 133 (4/4/21) Cited by 140 (4/6/22)

A 10-b 50-MHz CMOS D/A Converter with 75-Ω Buffer

MARCEL J. M. PELGROM, MEMBER, IEEE

Abstract—**A 10-b 50-MHz digital-to-analog (D/A) converter is presented which is based on a dual-ladder resistor string. This approach allows the linearity requirements to be met without the need for selection or trimming. The D/A decoding scheme reduces the glitch energy, and signal-dependent switch signals reduce high-frequency distortion. The output buffer allows driving 1 V_{pp} to 75 Ω. The chip consumes 65 mW at *maximum clock frequency and a full-swing output signal*. The device is processed in a standard 1.6-μm CMOS process with a single 5-V supply voltage.**

Current-based circuits dump the complementary part of the signal current to ground: the power supply current is thereby twice the average signal current. If a two-sided terminated transmission line has to be fed by the high-impedance output of the current cell D/A converter, the current should be doubled to obtain the required output swing. In this case, the power supply current is four times the average signal current. A triple video D/A converter

Pelgrom Paper Assessment

This paper proposes a trimless 10-b 50-MHz D/A converter based on resistor strings. This D/A converter is well suited to be used together with nearly all reported A/D converters for high speed, as these also use resistor strings to obtain the reference for the comparators. The design improves on the standard single-resistor-string approach by using a dual-ladder architecture [3] in a matrix formation [4], [5]. Several measures have been taken in the ladder to reduce the distortion. The decoding aims at minimizing the number of transistors that switch. The on-chip output buffer allows driving 1 V_{pp} to 75 Ω. The inherent voltage output allows driving a two-sided terminated transmission line with a better power efficiency than a current cell D/A converter.

Pelgrom Paper Assessment

II. The Chip Design

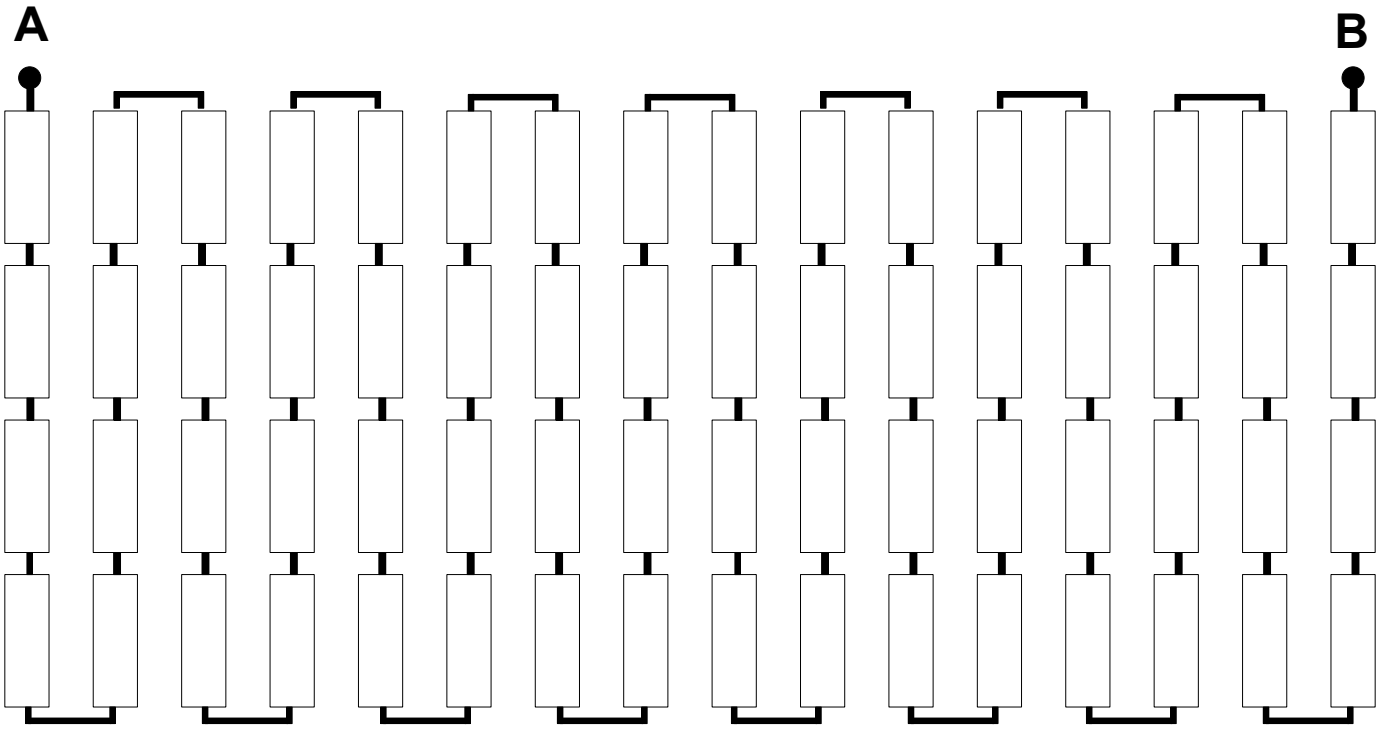
A. The Ladder Structure

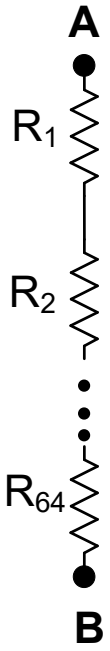
The voltage dependence and the mutual matching of large-area polysilicon resistors allow the design of a converter with high integral and differential linearity. Basically, the variation in the polysilicon resistance value is determined by its geometry variations: the length and width variations result in local mismatches and the thickness variation gives gradients. Equally sized MOS gates suffer in addition to charge variations in the threshold voltage. However, the design of the D/A converter with a single 1024-tap resistor ladder and sufficiently fast output settling requires tap resistors in the order of 6–10 Ω. The size of such resistors in conventional polysilicon technology is such that accurate resistor matching and consequently linearity become a problem.

Pelgrom Paper Assessment

The solution to this problem is the combination of a dual ladder [3] with a matrix organization Randy Geiger Fig. 1 shows the ladder structure. The coarse ladder consists of two ladders each with 16 large-area resistors of 250 Ω which are connected anti-parallel to eliminate the first-order resistivity gradient. The coarse ladder determines 16 accurate tap voltages and is responsible for the integral linearity. A 1024-resistor fine ladder is arranged in a 32-by-32 matrix, where every 64th tap is connected to the coarse-ladder taps. This arrangement allows the fine-ladder tap resistance to be increased to 75 Ω without loss of speed. The effect of wiring resistances has to be related to the 75-Ω tap resistors and can therefore be neglected. There are only currents in the connections between the ladders in the case of ladder inequalities: this reduces the effect of contact resistance variance. The current density in the polysilicon is kept constant to avoid field-dependent nonlinearities. The coarse ladder is designed with polysilicon resistors in order to avoid voltage dependence of diffused resistors. The fine ladder is designed either in polysilicon or diffusion, depending on secondary effects in the process implementation.

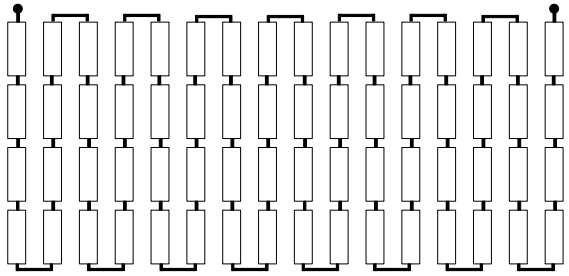
Resistor Layout

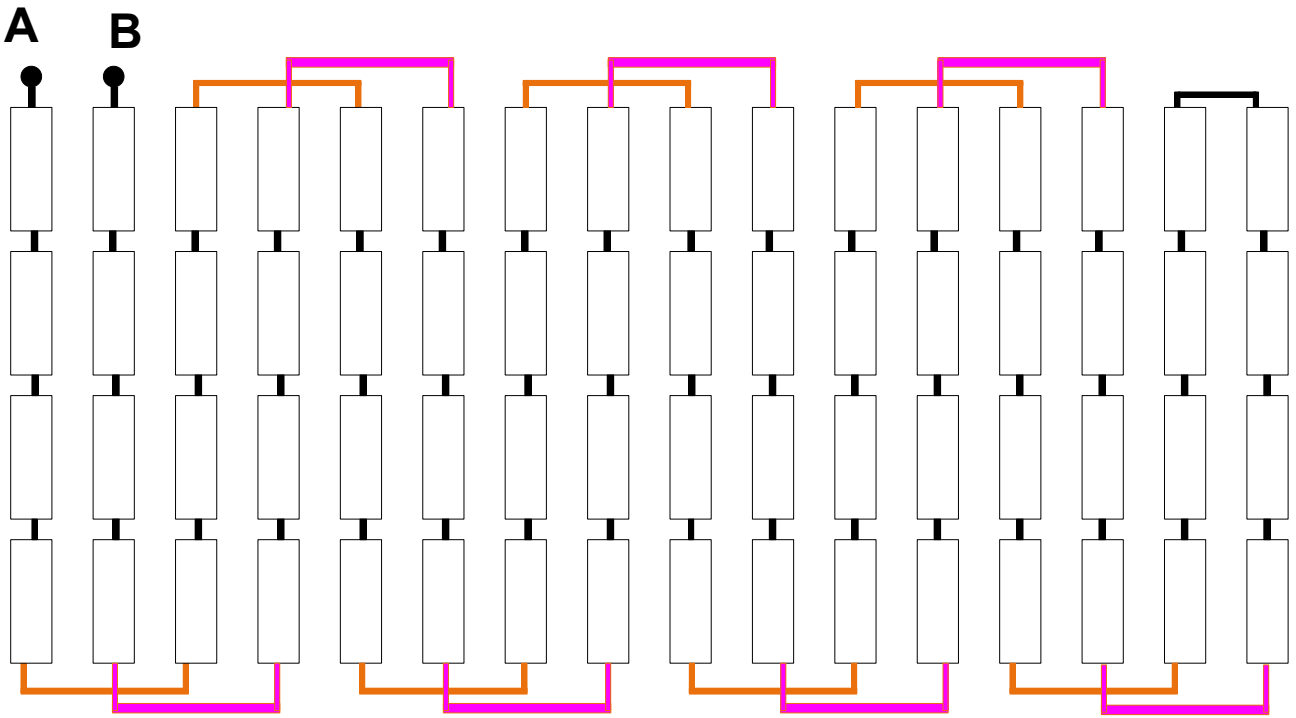


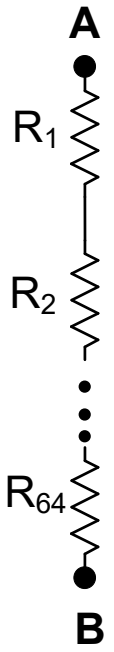


Standard Series Layout of 64 resistors

Resistor Layout

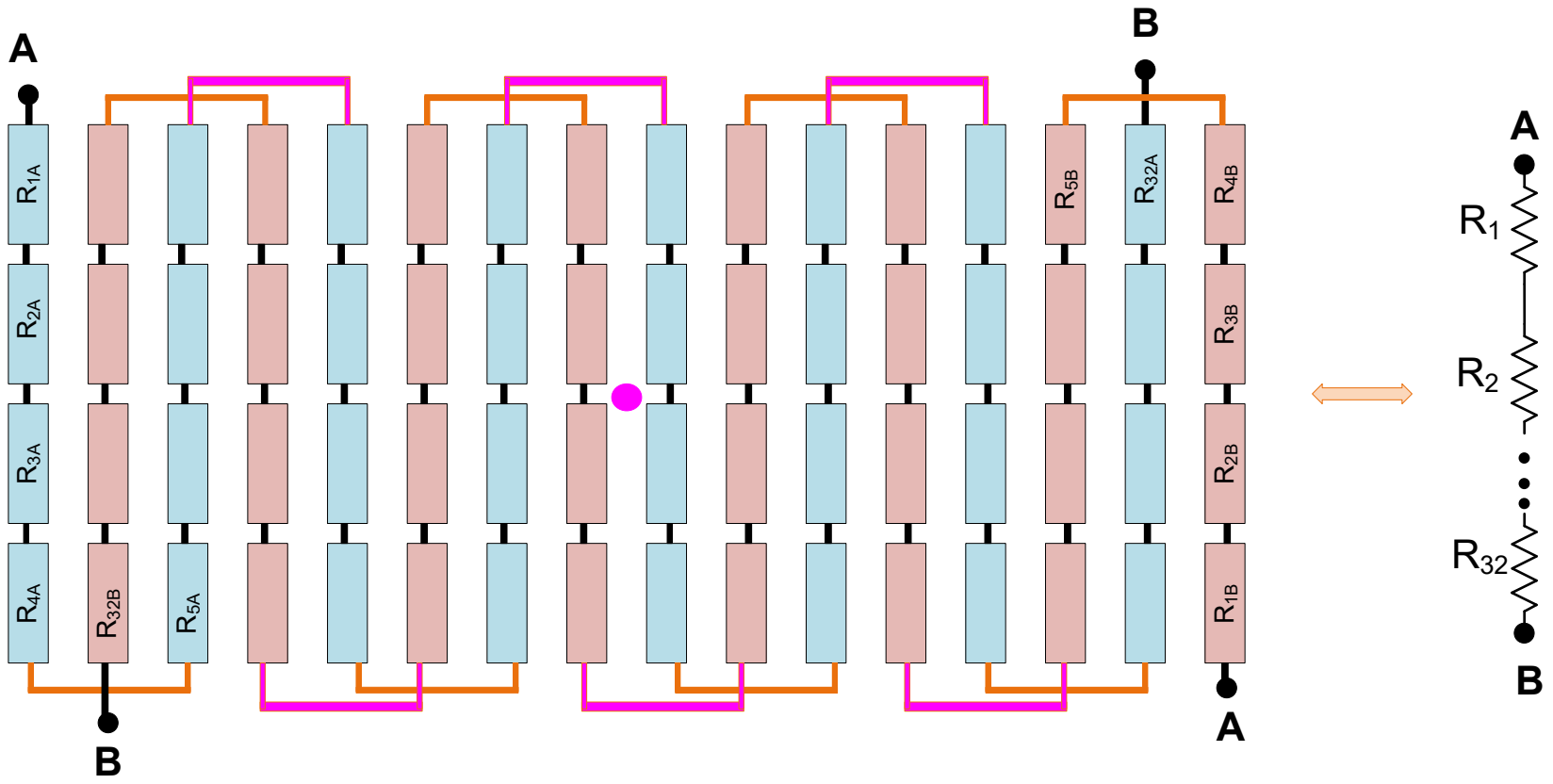






Layout of 64 resistors with reduced gradient sensitivity

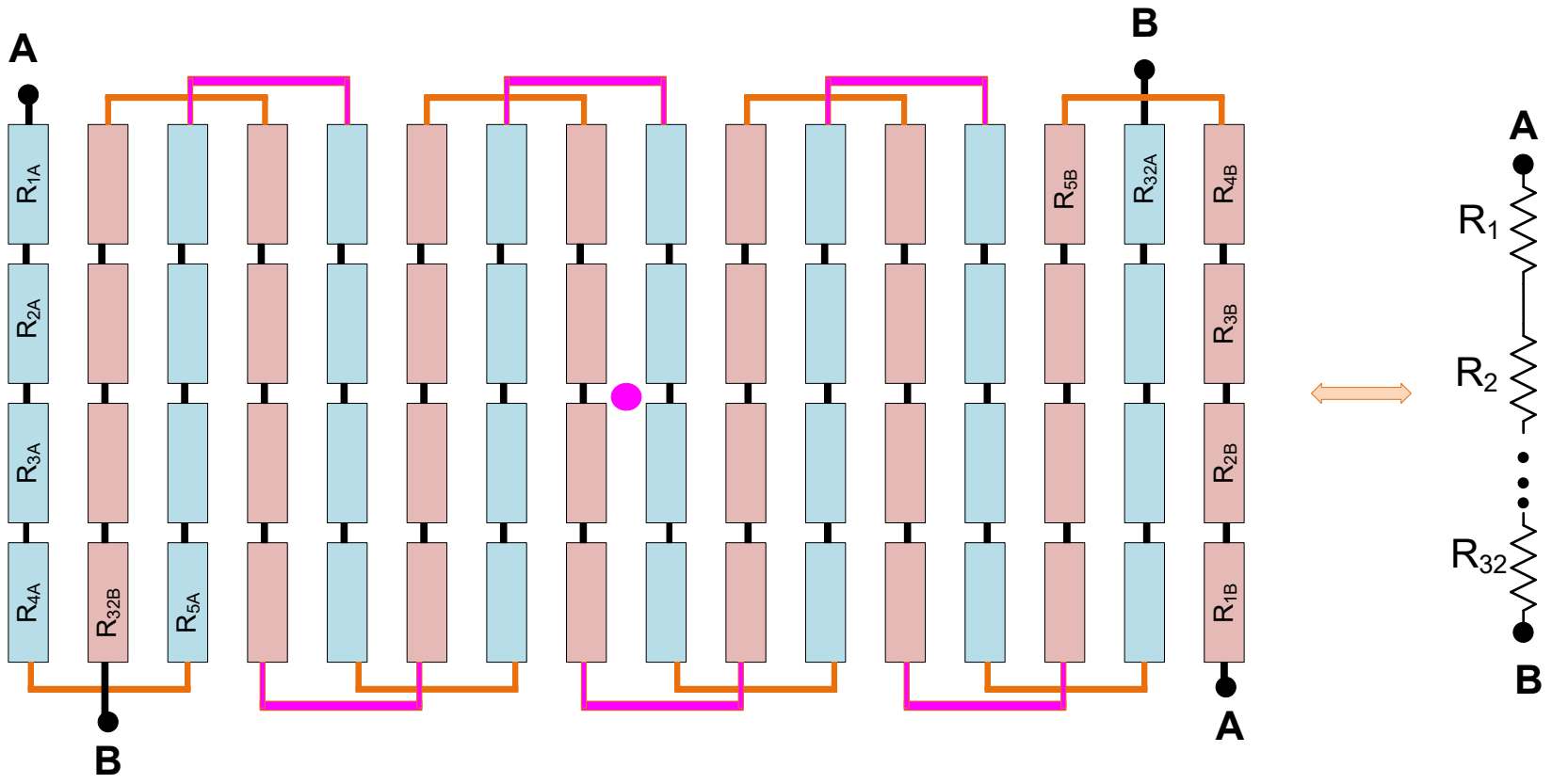
Resistor Layout



Antiparallel Layout of 32 resistors with Common Centroid

(Pelgrom used only 16 resistors)

Resistor Layout



Antiparallel Layout of 32 resistors with Common Centroid

Pelgrom Paper Assessment

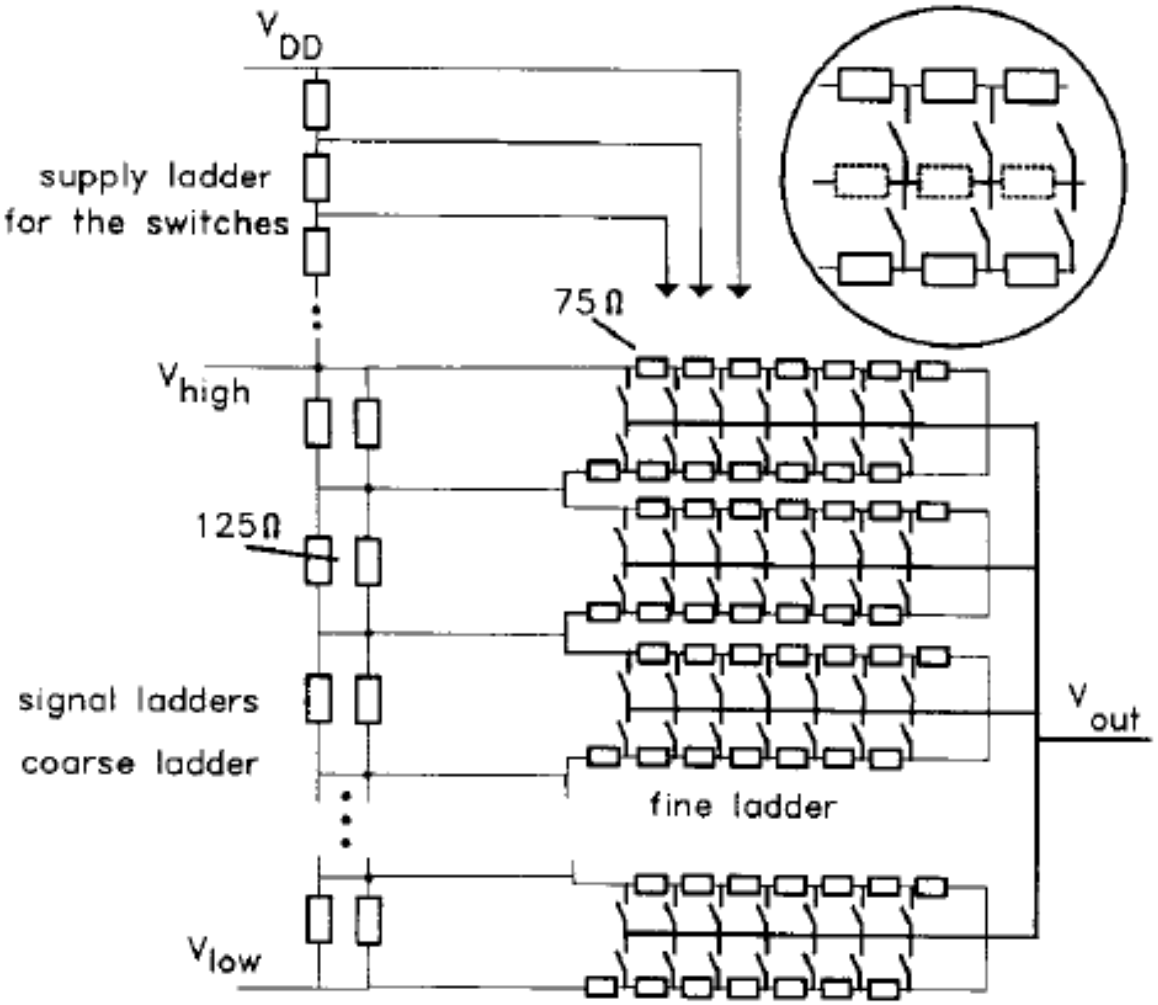


Fig. 1. Resistor network for the video D/A converter.

Pelgrom Paper Assessment

In a basic ladder design consisting of one string of 1024 resistors, the output impedance of the structure varies with the selected position on the ladder and therefore with the applied code. The varying output impedance in combination with the load capacitance results in unequal output charging time and consequently signal distortion of high-frequency output signals. This source of varying impedance has been eliminated by means of a resistive output rail. The insert in Fig. 1 shows a part of two rows of the matrix. Small resistors are placed in the output rail which connects the switches together. These resistors can be chosen in such a way that any path from the beginning of the resistor row to the end of the output rail shows the same impedance, independent of the chosen switch. This eliminates position-dependent charging of the output rail

Pelgrom Paper Assessment

and therefore reduces the odd harmonics. In this design, partial cancellation was achieved by placing a unity resistor at the appropriate positions in the output rail. The use of unity resistors keeps the layout simple and does not require additional chip area.

The second source of the varying output impedance is the switch transistor. Usually its on-state gate voltage equals the positive power supply; the voltage on its source terminal, however, is position dependent. The turn-on voltage doubles from one end of the ladder to the other. In this design an additional supply ladder is placed on top of the signal ladders to keep the turn-on voltage of the switches more constant. Effectively the turn-on voltage of each switch transistor is made equal to the lowest turn-on voltage of a basic ladder D/A structure. Therefore there are no additional power supply constraints. For an easy implementation, the switches along each output rail have a common supply line. The variation in turn-on voltage is thereby reduced by a factor of 16. The upper group of switches is fed from the power supply while each lower group is fed with a voltage lowered by one-sixteenth of the maximum signal swing. An additional advantage of this compensation is that the impedance of the switch can be in the order of the total ladder resistance: the switches reduce in width and consequently the clock feedthrough is also reduced.

Pelgrom Paper Assessment

B. The Digital Decoder

The core of the D/A converter is formed by the 32-by-32 fine-resistor matrix. A switch and a two-input AND gate[1] are connected to each fine resistor to form a basic cell. Two rows of 32 cells each are arranged around one output rail to form one of the 16 sections of the 10-b D/A converter (see Fig. 2). In operation one of the tap voltages of the fine ladder is switched to one of the 16 output rails of the matrix and subsequently to the input of the buffer. In order to select the proper switch, the 10-b digital input word is split in two 5-b words which are decoded by two sets of 5-to-32 decoders, as shown in Fig. 2. The 5-to-32 decoding is performed in two steps: a predecoder converts into ten lines that control 32 three-input NOR gates of which one gate is activated. In this way minimum capacitive load is driven and maximum speed is achieved. The two decoders are placed on two sides of the matrix. The two sets of 32 decoded lines are latched by the main clock before running horizontally and verti-

Pelgrom Paper Assessment

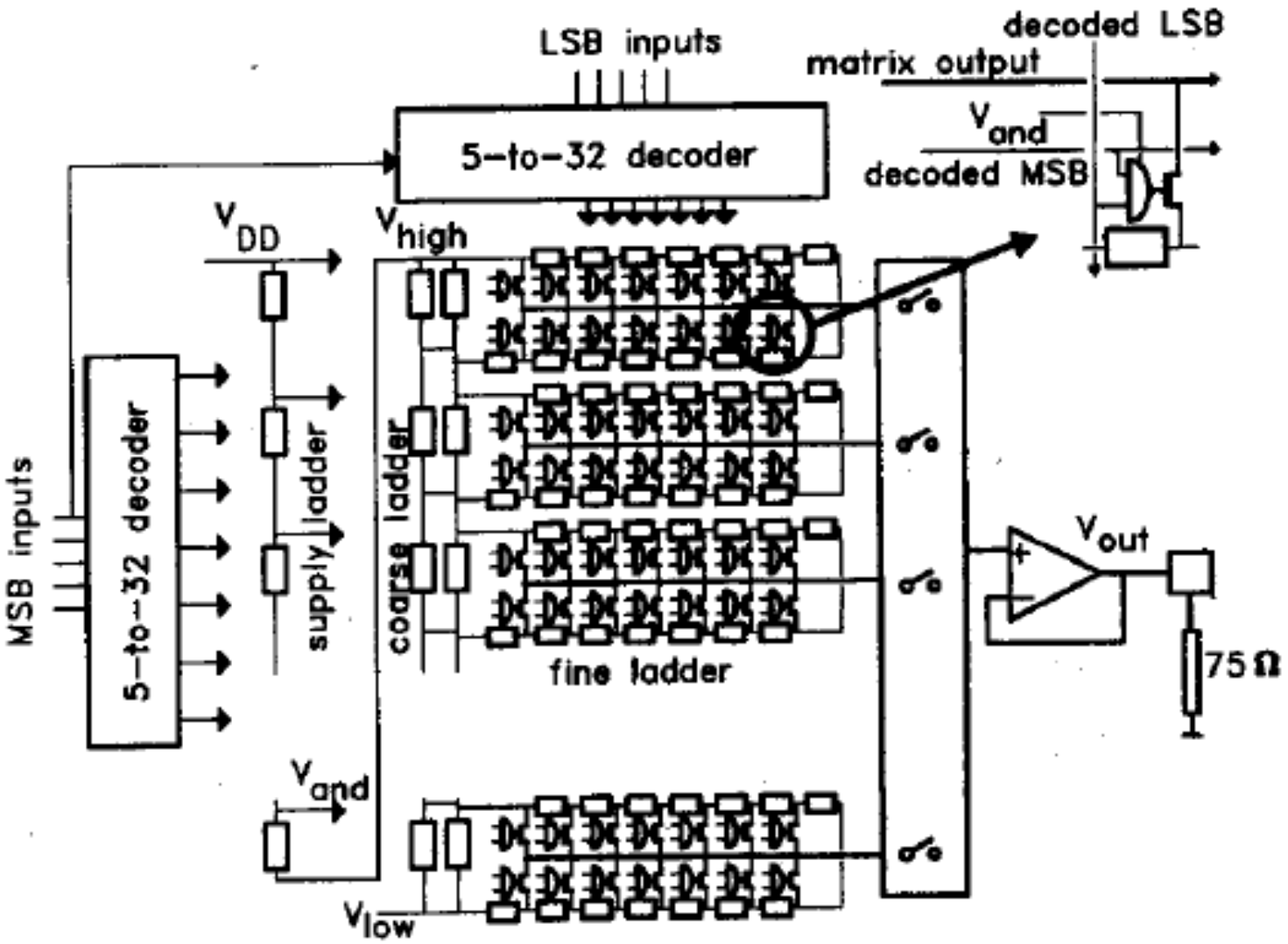


Fig. 2. Block diagram of the D/A converter.

Another key paper for matching-critical circuits:

Matching properties of MOS transistors [PDF] ieee.org

MJM Pelgrom, ACJ Duinmaijer… - IEEE Journal of solid …, 1989 - ieeexplore.ieee.org

The **matching properties** of the threshold voltage, substrate factor, and current factor of **MOS** transistors have been analyzed and measured. Improvements to the existing theory are …

☆ Save 99 Cite Cited by 4062 Related articles All 26 versions

2401 on Apr 7 2014

3452 on Apr 18 2018

3528 on Apr 17 2019

3745 on Apr 10 2020

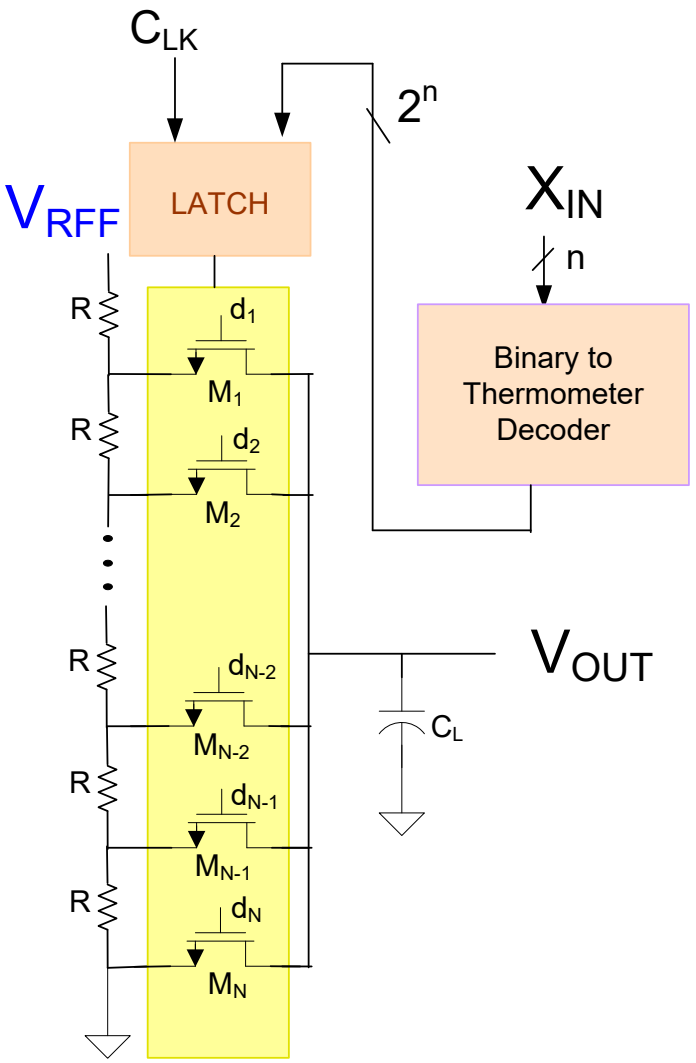
3913 Apr 4 2021

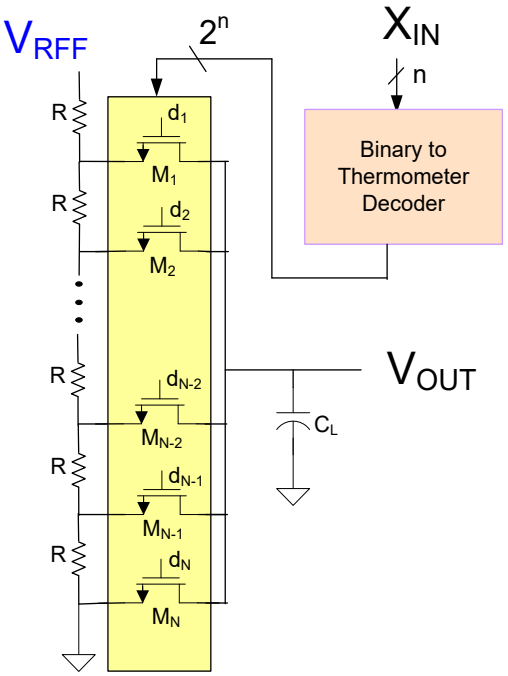
4062 Apr 6 2022

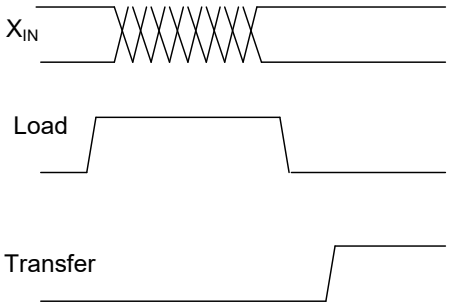
Second most cited paper in the IEEE Journal of Solid State Circuits

Most cited basic research paper in IEEE Journal of Solid State Circuits

Basic R-String DAC

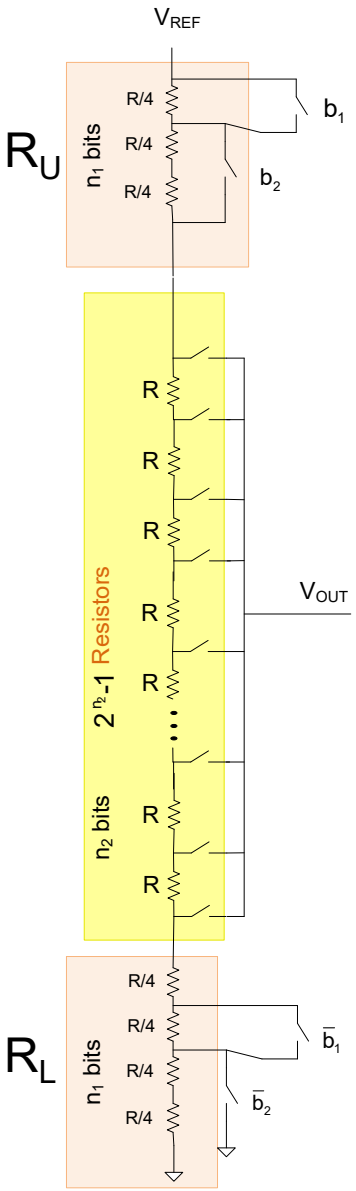






Latching Boolean Signal Can Reduce/Eliminate Logic Transients which Cause Distortion

Basic R-String DAC



For all b_1 and b_2, $R_U+R_L=R$

- Another Segmented DAC structure
- Can be viewed as a “dither” DAC
- Often n_1 is much smaller than n_2
- Dither can be used in other applications as well

Stay Safe and Stay Healthy !

End of Lecture 32